32.3 A PLL for a DVD×16 Write System with 63 Output Phases and 32ps Resolution

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Recently, interpolated ring oscillators have become popular [1]. A precise and high-resolution phase generation technique is needed for several signal processing applications. For example, the write circuitry for optical disks needs very high resolution phase information [2]. In order to create fine marks and spaces on the digital versatile disk (DVD), corresponding to several DVD standards, at least $T/40$ phase resolution is needed. Figure 32.3.1 shows the block diagram of the write circuitry for a DVD×16 system. The PLL, including a 63-phase ring-type current-controlled oscillator (ICO), provides enough clock phases for the pulse generation. Nine write pulses are sent to the write amplifier in the pick-up through the LVDS drivers.

Figure 32.3.2(a) shows the schematic of the 63-phase ring ICO. Each inverter output in the seven 9-stage inverter chains is connected to a different point in the 63-stage phase-coupled chain. The ring ICO outputs the phases of these 63 coupled points through buffers. We adopted a single-ended inverter to make the ICO as small as possible. The number of inverters in one ring and the number of the rings are chosen so that the product of these numbers is greater than 40 and both numbers are odd.

The oscillation frequency of the inverter chains is controlled by the supply current from a VtoI converter. All the PMOS source nodes in the inverter chains are connected together so that the oscillation frequency and amplitudes of all the inverter chains are the same. The phase couplers synchronize the phases of the inverter chains and the couplers compose the phase-coupled chain.

There are three options for coupling the phase of inverter chains as shown in Fig. 32.3.2. If an inverter is used for phase coupling as shown in Fig. 32.3.2(b), the ICO has a lower limit of oscillation because the phase-coupled chain oscillates by itself. Thus, using the inverter for phase coupling is not suitable for a DVD, which requires wide oscillation range from DVD×1 to DVD×16. Figure 32.3.3(a) explains the operation of the NMOS forward phase coupler shown in Fig.32.3.2(c). P_n is the oscillation waveform of the 0^{th} inverter chain and P_{n+1} is that of $(n+1)^{st}$ inverter chain, respectively. The rising edge of P_{n+1} is delayed while P_n is high because the coupling transistor decreases the supply current to the gate capacitance of the next inverter. On the other hand, the falling edge of P_{n+1} is advanced by the transistor while P_n is high. Thus, the phase of P_{n+1} is locked 180 degrees out of phase with P_n. The accurate lock position of the output of the n^{th} inverter in the m^{th} inverter chain, $P_L(n,m)$, is given by the following equation.

$$P_L(n,m) = m\times(180+360/(2n_{inv}\times n_{ch})) + n\times(180+360/(2n_{imv}))\bmod 360 \quad (1.1)$$

Here, n_{inv} is the number of the inverters in the ring and n_{ch} is the number of inverter chains, respectively [3].

The acquisition characteristic of the NMOS forward coupler is shown in Fig. 32.3.3(b). By coupling the phase, the NMOS forward coupler changes the oscillation frequency of the ring oscillator by $\Delta F_c(\theta_e)$ as compared to the frequency without the phase coupling. The phase difference between P_n and P_{n+1} is represented by θ_e. Having a wide acquisition range is desirable for a ICO in deep submicron processes, because the variation of the free-running frequency of each inverter is large due to the large shallow trench isolation (STI) stress. Making the size of the coupling transistor larger in the NMOS forward coupler actually widens the frequency acquisition range. However the accuracy of the interpolation is degraded due to the decrease in the size of the linear region of frequency acquisition. On the other hand, the NMOS latch coupling, as shown in Fig. 32.3.2(d), doubles the range of acquisition without decreasing the linearity, because the number of operations for the acquisition of the NMOS latch is twice that of the NMOS forward coupler. The latch operation does not decrease the linear region for the phase interpolation. Therefore, the NMOS latch gives the best performance for phase coupling.

The origin of the multiphase oscillator is the array oscillator reported by Maneatis [3]. Although the array oscillator has good performance, the area of the oscillator is quite large because it requires multiple power supply lines. Moreover, a large oscillator makes it difficult to realize multiple outputs whose timings are the same. In order to realize the small multiphase ring oscillator, we have adopted a new layout method. Figure 32.3.4(a) illustrates a part of the schematic of the 63-phase ring ICO. The transistors which have a common input gate compose a unit cell. The unit cell has a very thin shape and a small area. The output of the inverter in each unit cell is connected to the input of the 7th following cell. The phase coupler connects the neighboring unit cells. Figure 32.3.4(b) shows the block layout of the ICO. The ring ICO is divided into two blocks; one block includes 32 unit cells and the other includes 31 block cells. The two blocks are placed in parallel. Careful routing of the wires is required to minimize bulges. In this layout, we need far fewer power lines than an array oscillator would. Thus, a very small multiphase ring oscillator is realized. Neither a column nor row selector is needed. All phase information is directly fed to the level shifters. Moreover, the new layout method is applicable to every multiphase ring oscillator. Whatever phase ring oscillator you may fabricate, the same unit cell can be used.

The test chip is fabricated in a 65nm CMOS process with 7 metal layers. The chip micrograph is shown in Fig. 32.3.7. The size of the 63-phase ring oscillator is only 36μm×46μm. The PLL can output the multiphase write pulses from 24.8MHz (DVD×1) to 490MHz (DVD×16). The measured performance of the PLL is summarized in Fig. 32.3.6. The measured period jitter at 490MHz output was 3.47psec and accumulated jitter was 13.7psec, respectively. The period jitter is small enough not to affect the write pulse generation because it is about 1/10 of 1.0LSB resolution of the phase (32psec). The DNL characteristic at 490MHz is shown in Fig. 32.3.5. The DNL measured at the output of the LVDS drives was within ±1.0LSB (from -1.0 to 0.8). A phase resolution of 32psec has been successfully achieved with small power (17mW) by using a compact layout method in a 65nm process.

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[2] Yoshiaki Konno, et al., "A CMOS 1×-to 16×-Speed DVD Write Channel IC," *IEEE ISSCC Dig. Tech. Papers*, pp.568-569, Feb., 2005.
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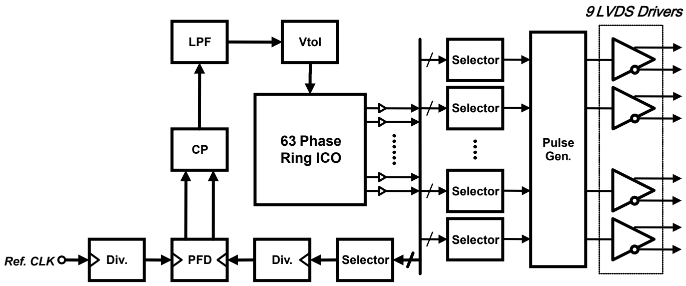

Figure 32.3.1: Block diagram of write circuitry.

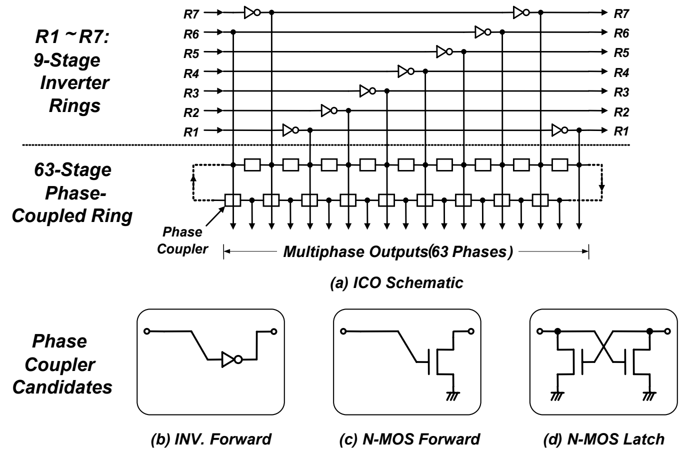

Figure 32.3.2: Schematic of the 63-phase ring ICO.

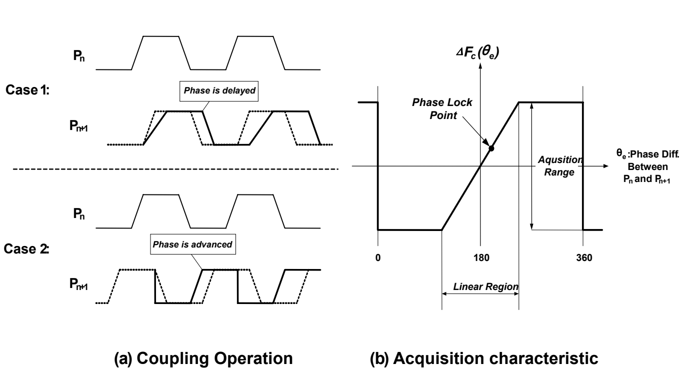

Figure 32.3.3: Principle of the phase coupler.

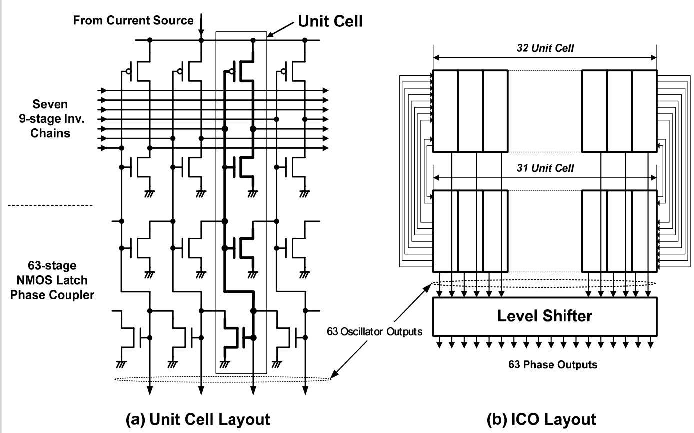

Figure 32.3.4: Layout method for ring oscillator.

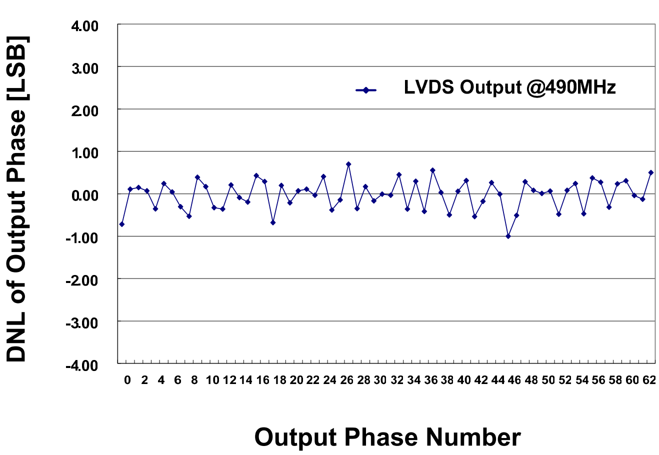

Figure 32.3.5: Measured DNL of the output pulses.

Output Frequency		24.8-490MHz (DVDx1-x16)
Phase Resolution		T/63(>32psec)
DNL of Output Phase		-1.0 ~ 0.8LSB@490MHz
Period Jitter(3σ)		3.47psec(0.17%)@490MHz 25.6psec(0.067%)@26.17MHz
Accumlation Jitter(3σ) (3000Clocks)		13.7psec(0.67%)@490MHz 84.1psec(0.22%)@26.17MHz
Power Consumption	Analog Digital	17mW@490MHz 22mW@490MHz

Figure 32.3.6: Measured chip performance.

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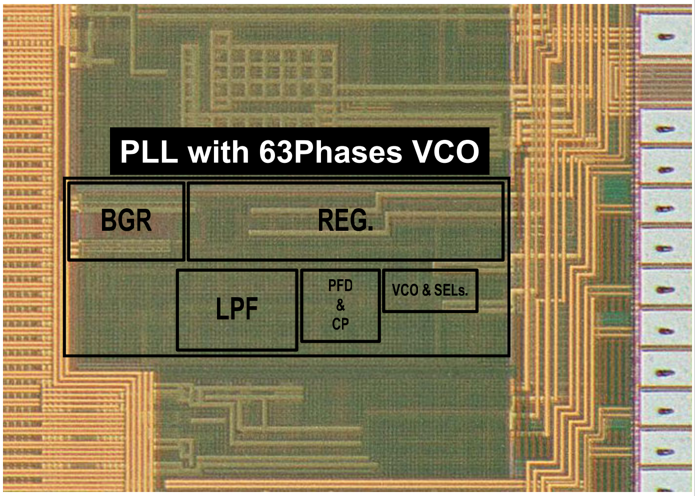

Figure 32.3.7: Micrograph of the PLL with 63 phases VCO.